REMARKS

Claims 82 and 83 have been amended. New claims 94-97 have been added. No new matter has been introduced by the amendments. Claims 39, 41-46, 48, 50-55, 74-83, and 94-97 are pending in the application (herein referred to as the "'132 application"). Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 39 and 41-46 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Laibowitz et al., U.S. Patent No. 6,088,216 (hereinafter "Laibowitz"), in view of Azuma et al., U.S. Patent No. 5,516,363 (hereinafter "Azuma"). The rejection is respectfully traversed.

Claim 39 recites a capacitor having a "first level and a second level" connected by "at least two sidewall regions." The recited capacitor also includes "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." According to the claim, the ion implantation doped BST high dielectric constant thin film material is "a continuous layer at least on said two sidewall regions and said second level." Applicant respectfully submits that Laibowitz and Azuma do not teach or suggest the claimed invention.

Laibowitz discloses a three-dimensional (3D) DRAM capacitor comprising a substrate 12, whereupon a mesa 51 and high dielectric film 56 are formed (Figure 7). Laibowitz, however, fails to teach or suggest a capacitor in which the stoichiometry of the sidewalls is substantially uniform, as recited in claim 39. Laibowitz discloses a thin film material deposition technique and resulting structure upon which the claimed invention improves.

Laibowitz discloses a "[h]igh dielectric constant material 66 [] *deposited* to form dielectric layer 67 having a predetermined thickness." (Col. 3, lines 43-45) (emphasis added). Although Laibowitz fails to state which deposition technique it uses to deposit the high dielectric constant material, it is well known in the art that these materials are generally deposited by chemical vapor deposition (see '132 application, page 2, line 12 to page 3, line 8) or conventional sputtering techniques (see '132 application, page 8, lines 7-9). CVD techniques suffer from inhomogeneity in stoichiometry on sidewalls of 3D structures. (See '132 application, page 3, lines 9-10). Similarly, conventional sputtering techniques result in clumped areas of massed materials having non-uniform thicknesses and stratified layers that are improperly mixed to <u>non-homogenous</u>, i.e., non-uniform, proportions that are incapable of forming proper average crystals on sidewalls of either trenches or studs. (See '132 Application, page 8, lines 7-9).

Because Laibowitz uses conventional techniques of forming its dielectric layer 56 on a sidewall, Laibowitz fails to disclose a capacitor having "an ion implantation doped BST high dielectric constant thin film material having substantially uniform stoichiometry formed over [] at least two sidewall regions," as recited in claim 39.

Azuma relates to a method of achieving uniform stoichiometry. Specifically, Azuma discloses a method of spin-coating a dielectric thin film precursor on a substrate. (Col. 18, lines 3-7). Referring to FIG. 3, reproduced below, Azuma discloses a method of fabricating the illustrated capacitor 10 by fabricating a substrate 18, which includes layers 11, 12, 13, and 14. (Col. 17, lines 45-48). A standard BST solution is prepared, and subsequently doped to form the BST precursor. (Col. 17 line 65 through Col. 18, line 1). The precursor solution is applied to the substrate 18, "by dropping the precursor solution onto substrate 18 and then spinning substrate 18 at about 1500 RPM (the preferred range is about 1500-2000 RPM) for about 30 seconds." (Col. 18, lines 4-8). The BST precursor is then dried and annealed to form a metal oxide dielectric material

15 on substrate 18. (Col. 18, lines 8-11). A second electrode 16 is then formed atop the dielectric layer 15. (Col. 18, lines 33-34).

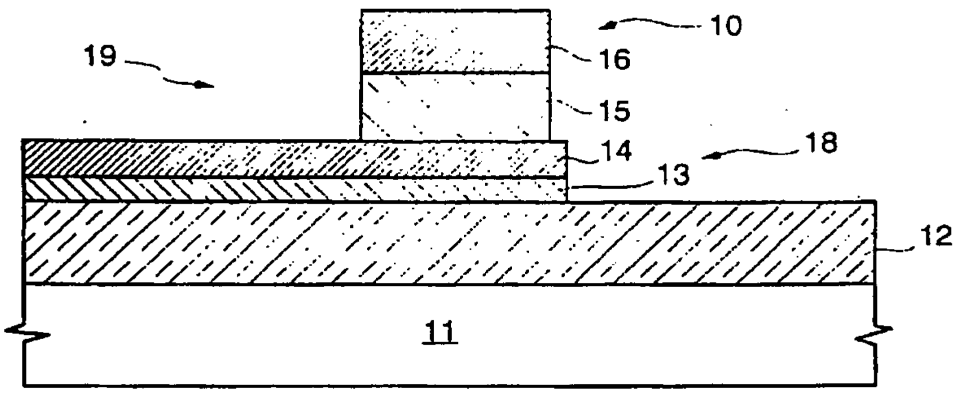


FIG. 3

Azuma fails to disclose a "material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels," as recited in claim 39. Indeed, each layer 11, 12, 13, 14, 15, 16 of Azuma's FIG. 3 capacitor is formed on top of a preceding layer having a topmost surface located on a <u>single</u> level. For example, layer 15 is formed over layer 14 having a topmost surface on a <u>single</u> level not having any sidewall regions. Azuma's method of spin-coating the precursor solution forms a dielectric thin film material having only a single level, without sidewall regions. For at least this reason, Azuma fails to teach or suggest "an ion implantation doped BST high dielectric constant thin film material having substantially uniform stoichiometry formed over [] at least two sidewall regions," as recited in claim 39.

The Office Action asserts that Azuma and Laibowitz are properly combinable because the two references "clearly apply to the same art." (Office Action, page 5). The Office Action further states that "it is not expected necessarily that exactly the same

method used in Azuma must also be applied to the structure of Laibowitz." (Office Action, page 5).

Applicant respectfully disagrees with the Office Action's assertions. First, Laibowitz relates to the art of depositing a dielectric thin film on a 3D substrate by conventional techniques such as sputtering or CVD, as discussed above. Azuma, on the other hand, relates to the art of spin-coating a dielectric thin film material on a substrate, as discussed above. Therefore, the two references do not apply to the same art.

Second, even if the two references apply to the same art, which they do not, the two references are not properly combinable because, as discussed below in further detail, the same method used in Azuma (i.e., spin-coating) cannot be applied to the structure of Laibowitz. Similarly, the method of deposition used by Laibowitz cannot be applied to a 3D structure using Azuma's precursor solution. Because the only workable method of applying the Azuma precursor solution onto the 3D structure of Laibowitz is by spin-coating, as will be discussed in further detail below, the two references cannot be combined.

Because the two references are not properly combinable, the subject matter of claims 39 and 41-46 would not have been obvious over Azuma in view of Laibowitz. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir.

1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

As noted in the attached Declaration of Garo Derderian, Senior Engineer in the Process Development Group of Micron Technology Inc.'s Research and Development Department, the Azuma and Laibowitz references are not inherently combinable. Dr. Derderian's Declaration establishes that as of the filing date of the current application, a person having ordinary skill in the art of CVD deposition of metals would be a person with at least a Masters degree in Materials Science and Engineering and with at least three (3) years processing experience in the deposition processes of the semiconductor industry. Additionally, as of the filing date of the current application, a person having ordinary skill in the art of spin-coating techniques, or wet-techniques, would be a person with at least a Masters degree in Material Science and Engineering and with at least three (3) years processing experience in spin-coating deposition processes.

Dr. Derderian has been engaged in the research and development of film deposition and film treatment processes used in semiconductor manufacturing. In particular, Dr. Derderian has worked on various developmental projects regarding the chemical vapor deposition (CVD) of metals and oxides, including high constant dielectrics for DRAM manufacturing. As a result, Dr. Derderian is knowledgeable as to what persons of ordinary skill in the art would have known and understood relating to the chemical vapor deposition processes in semiconductor processing as of August 2000.

Additionally, Dr. Derderian has had at least three years of experience in wet-techniques; specifically, spin-coating sol-gel materials onto substrates. Indeed, a portion of Dr. Derderian's dissertation involved the spin-on deposition of sol-gel potassium niobium oxides. Consequently, Dr. Derderian is knowledgeable as to what

persons of ordinary skill in the art would have known and understood relating to the spin-coating processes in semiconductor processing as of August 2000.

As established by the Declaration, Dr. Derderian's understands that those of ordinary skill in the art would not use techniques such as spin-coating with 3D structures. Moreover, Dr. Derderian's Declaration establishes that there is no motivation in either the references themselves, or in the knowledge of a person of ordinary skill in the art to combine the two references. Additionally, there is no likelihood of success that the combination of the two references would result in the claimed invention.

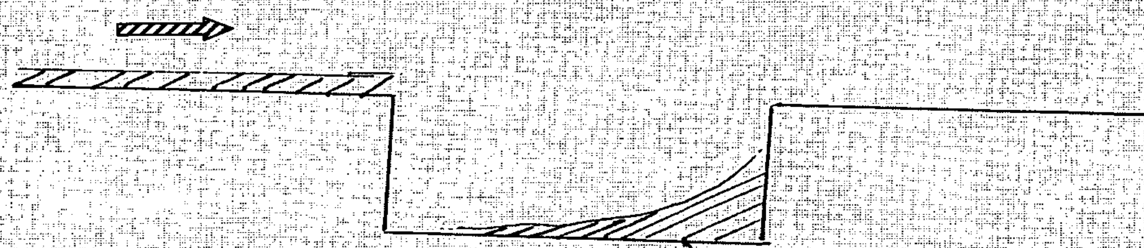
First, as illustrated by FIGS. A and B, the combination of Azuma and Laibowitz would result in an unworkable capacitor. Referring to Fig. A, the spin-coat method disclosed by Azuma would result in an accumulation of the pre-doped precursor solution on a near raised sidewall, while not covering the far raised sidewall at all.

FIG. A.

(STOD)

In the case of a deep trench (Fig. B), the pre-doped precursor solution would accumulate at the far lowered sidewall, while failing to cover the near lowered sidewall. Therefore, the combination of using Azuma's spin-coating technique on Laibowitz' 3D structure would not result in a "continuous layer" over two sidewall regions and a second level, as recited in claim 39.

FIG. B



(TRENCH)

The process of spin-coating the high dielectric thin film precursor would result in an unworkable capacitor because the failure to achieve 100% step coverage by spin-coating would open the circuit in which the capacitor is a part since there is a discontinuous layer.

Second, as confirmed by Dr. Derderian, Azuma's precursor solution cannot be deposited by using Laibowitz' conventional techniques. For example, it is well known in the art that solutions cannot be used with conventional sputtering techniques. Azuma's precursor solution cannot be deposited by CVD techniques either. Azuma's precursor solutions, like many solutions used in wet-techniques, are formed by mixing high constant dielectric thin film materials with solvents to make an aqueous solution. (See e.g., Azuma Col. 6, lines 60-67). Because the solvents typically have a higher vapor

pressure as compared with the high dielectric constant thin film materials, it is not practical to deposit the Azuma liquid precursor by CVD. Because the vapor pressure of the high dielectric materials is low, while the vapor pressure of the solvents is high, the solvents would first vaporize leaving the high dielectric thin film materials behind. In addition, the temperature with which to vaporize the precursors would be too great for the high dielectric constant materials resulting in their decomposition. Therefore, the Azuma precursor solution could not be deposited by CVD. Even if it were to be deposited by CVD, the resulting structure would not have substantially uniform stoichiometry on the sidewall regions of a 3D substrate, as discussed above with respect to Laibowitz.

Additionally, wet-techniques are problematic in achieving thin films that are suitable for 3D DRAM capacitors, which require much thinner thin films than do flat capacitors. Flat capacitors, such as that disclosed by Azuma, typically have thin films in the range of approximately 1400Å to approximately 2000Å. For example, Table 5 of Azuma describes a range of dielectric thicknesses from 1440Å to 1840Å. 3D capacitors require significantly thinner thin films; typically requiring a dielectric thin film less than 100Å. For example, Laibowitz discusses a DRAM circuit in development that "uses a trench capacitor" having a dielectric thin film, wherein "[t]he dielectric thickness is about 7 nm," or 70Å. (Col. 1, lines 19-23). Wet-techniques, such as the spin-coating technique of Azuma, often achieve minimal thicknesses of only a few hundred angstroms (e.g., 500Å). The spin-coating technique <u>cannot</u> be combined with 3D structures, such as the Laibowitz capacitor, because the wet-technique cannot achieve minimal thicknesses required by the 3D structure of Laibowitz.

Finally, as explained by Dr. Derderian, there are density problems that arise with wet-techniques, such as the spin-coating disclosed by Azuma. Specifically, wet-techniques fail to achieve uniform densities, oftentimes creating pinholes or pores in the layers which they provide. Because the high dielectric constant thin film materials are

carried in liquid precursor solutions by adding solvents, heat must be applied to the substrate after the precursor solutions have been spin-coat as to remove the solvent from the surface of the substrate. After removing the solvent, however, pinholes are created, leaving uneven densities of high dielectric constant thin film material on the substrate. A means of creating more uniform densities has been to apply several coats of a liquid precursor, and heating the substrate in between each coat. Indeed, this is the method Azuma discloses. (See Col. 18, lines 9-19). The process of coating and heating achieves a more uniform density of the high dielectric thin film material, but also increases the thickness of the layer. The failure of wet-techniques to achieve uniform densities on flat surfaces at minimal thicknesses is greatly exaggerated when using wet-techniques on 3D structures, such as the structure disclosed by Laibowitz in FIG. 7. Therefore, as confirmed by Dr. Derderian's Declaration, those skilled in the art would not combine the subject matter of the two references cited by the Office Action, because it is illogical and unworkable.

Because it is well known in the art that wet-techniques are poor candidates with which to create thin films for 3D DRAM structures, there is no likelihood of success that the combination of Azuma and Laibowitz would result in the claimed invention. Applicant respectfully submits that Laibowitz and Azuma are not properly combinable.

Even if combinable, the two references fail to teach or suggest a capacitor having "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level" and being "a continuous layer" because Azuma involves a spin-coat step. As discussed above with respect to the combination of Azuma and Laibowitz, and as confirmed by Dr. Derderian, a spin-coating technique used on a 3D structure cannot result in a continuous layer.

Claims 41-46 depend from claim 39, and are allowable along with claim 39 for at least the reasons set forth above. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 48 and 50-55 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Laibowitz, in view of Azuma, and further in view of Leung et al., U.S. Patent No. 5,563,762 (hereinafter "Leung"). The rejection is respectfully traversed.

Claim 48 recites a capacitor having a "first level and a second level" connected by "at least two sidewall regions." The capacitor includes "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." According to the claim, the ion implantation doped BST high dielectric constant thin film material is "a continuous layer at least on said two sidewall regions and said second level." A capping layer is also provided over at least a portion of said BST thin film material.

As noted above with respect to claim 39, Laibowitz and Azuma are not properly combinable. Even if combinable, the two references fail to teach or suggest a capacitor having "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level; wherein said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions." Leung discloses preparation of a capacitor whereby "a capping layer is deposited overall to encapsulate the capacitor structure" (Col. 2, line 46-49). Leung does not, however, disclose a capacitor with uniform stoichiometry of the BST high dielectric constant thin film material. Accordingly, the combination of Laibowitz, Azuma and Leung fails to teach or suggest the subject matter defined in claim 48. For at

least the foregoing reasons, claim 48 is allowable over the combination of Laibowitz, Azuma, and Leung.

Claims 50-55 depend from claim 48, and are allowable along with claim 48 for at least the reasons set forth above. Accordingly the rejection should be withdrawn and the claims allowed.

Claims 74-83 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hosotani et al., U.S. Patent No. 6,051,859 (hereinafter "Hosotani") in view of Azuma. The rejection is respectfully traversed.

Claim 74 recites a capacitor having a first electrode having two sidewall regions and a second level and "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." The claim further recites that the ion implantation doped BST high dielectric constant thin film material is "a continuous layer at least on said two sidewall regions and said second level." A second electrode is provided on the BST high dielectric thin film material.

Hosotani discloses a cup-shaped capacitor comprising a substrate, first electrode, dielectric film, and second electrode. (FIG. 7B and Col. 12, lines 31-44). Hosotani discloses the deposition of the dielectric thin film material by CVD. (Col. 11, lines 64-65). As discussed above with respect to Laibowitz, CVD techniques suffer from inhomogeneity in stoichiometry on 3D structures. Indeed, even Hosotani admits that "the dielectric film is <u>anomalously</u> grown by the CVD method." (Col. 11, lines 64-65). For at least the foregoing reason, Hosotani fails to teach or suggest an ion implantation doped BST thin film material having a substantially uniform stoichiometry.

As discussed above with respect to claim 39, Azuma is not properly combinable with a 3D structure (e.g., the Hosotani cup-shaped capacitor). Even if

combinable, the two references fail to teach or suggest a capacitor comprising "a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions" and "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level" that is "a continuous layer at least on said two sidewall regions and said second level," as recited in claim 74. For at least the foregoing reasons, claim 74 is allowable over the combination of Azuma and Hosotani.

Claims 75-83 depend from claim 74, and are allowable along with claim 74 for at least the reasons set forth above. Accordingly the rejection should be withdrawn and the claims allowed.

New claim 94 recites a capacitor having a "first level and a second level" connected by "at least two sidewall regions." The capacitor includes "an ion implantation doped high dielectric constant thin film material, said ion implantation doped high dielectric constant thin film material having a general formula of ABO_3 and having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." According to the claim, the ion implantation doped high dielectric constant thin film material is "a continuous layer at least on said two sidewall regions and said second level."

As discussed above with respect to claim 39, Laibowitz and Azuma are not properly combinable. Even if combinable, the two references fail to teach or suggest a capacitor having a "continuous" "ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." For at least the foregoing reasons, claim 94 is allowable over the combination of Laibowitz and Azuma.

Similarly, as discussed above with respect to claim 74, Hosotani and Azuma are not properly combinable. Even if combinable, the two references fail to teach or suggest a capacitor having a "continuous" "ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." For at least the foregoing reasons, claim 94 is allowable over the combination of Hosotani and Azuma

Claims 95-97 depend from claim 94, and are allowable along with claim 94 for at least the reasons set forth above.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: January 12, 2003

Respectfully submitted,

By ____________________

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